Amendment to the Specification:

Rewrite the first paragraph on page 1 to read as follows:

This application claims priority to European Application Serial No. 00402331.3, filed August 21, 2000 (TI-31366EU) and to European Application Serial No. 01401678.6, filed June 25, 2001 (TI-32234EU). US Patent Application Serial No. [[_____]] 09/932,651, filed August 17, 2001 (TI-31366US) is incorporated herein by reference.

Rewrite paragraph number 30 to read as follows:

[30] Figure 6 is a more detailed block diagram of a portion of the digital system of Figure 2 that illustrates the usage of task-ID information for improved fault management and recovery from memory access errors. As described previously, CPU 105 has an instruction cache ~~106~~ 206 and data cache ~~102~~ 202 and additional local memory RAM. Memory requests to external memory 112 pass through level 2 interface 210 and traffic controller 110. When data is cleaned from data cache ~~102~~ 202, write buffer 650 is used to queue write requests to external memory 112. Task-ID information 670 is maintained within processor 105 and is updated by the operating system during context switch prior to a task execution. The task-ID information is also provided by task-ID register 670 to interface circuitry 210 and thence to traffic controller 110, μTLB 217, and write buffer 650 along with each memory request via signals 672.